NAME: _____ (FIRST NAME FIRST) **SCORE**: _____

COSC 3330 FINAL EXAMINATION MAY 7, 2010

*This exam is **closed book**. You can have **one page** of notes. UH expels cheaters.*

1. A virtual memory system has 64-bit addresses and a page size of 16 kilobytes. How many bits of the address are used by

a. The ***byte offset***? (5 points) **Answer:** $\log_2(16K) = 14$ **bits**

b. The ***page number***? (5 points) **Answer:** 64 - 14 = 60 **bits**

2. Which particularity of the x86 Intel/AMD architecture complicates the task of implementers of virtual machine support software? (5 points)

The whole VM approach assumes that a kernel executing in user mode will behave exactly like a kernel executing in privileged mode except that privileged instruction will be trapped.

This is not true for the Intel x86 architecture: Pop flags (POPF) instruction

3. A computer system achieves 99.5 percent availability with a repair time of 12 hours. What is its mean time to failure? (5 points) (*Hint: express your answer in days*.)

The MTTF of the system is 99.5 days

Starting with $A = MTTF/(MTTF + MTTR)$, we have
$MTTF = A/(1-A) \times MTTR = 0.995/(0.005) \times 0.5 = 0.995 \times 100 = 99.5$

4. Your employer is thinking of purchasing either a shared memory multiprocessor or a computer cluster for performing huge simulations. What are the ***respective disadvantages*** of the two solutions? (2×5 points)

Shared memory multiprocessors are easier to program.

Computer clusters are cheaper and very easy to assemble but all data exchanges among computers must be done through message passing.

5. A small direct-mapping cache has 2,048 entries with each entry containing four words. The computer memory is byte-addressable and all addresses are 32-bit addresses. (4×5 points)

a. What is the ***cache size*** (tags excluded) in ***bytes***? **Answer:** $2{,}048 \times 4 \times 4 = 32K$ **bytes**

b. What is the ***tag size*****?** **Answer:** 32 – 4 – 11 =17 **bits**
(*You can use this space to detail your computation*.)

Remove $\log_2(16) = 4$ bits since of each entry is 16-byte long and
$\log_2(2{,}048) = 11$ bits that are given by address in cache.

c. How could we increase the ***hit ratio*** of the cache ***without increasing its size*****?**
(*You do not need to describe how you would implement your solution.*)

Replacing it with a set-associative cache that could store 1,204 pairs of four-word entries.

d. What would be the ***main disadvantage*** of your solution**?**

Set-associative caches are slower than direct mapping caches.

6. ***Caches and virtual memory:*** (4×5 points)

a. What would be a ***reasonable page size*** for a ***virtual memory system***? **Answer:** 4K **bytes**

b. Justify your answer in a few words.

Because page faults are very costly, the system should try to bring in as many useful data as possible.

c. Would that be a ***reasonable block size*** for a cache? **YES** ____ **NO** _X__

d. Justify your answer in a few words.

Cache block sizes are much smaller: 64 bytes is a good choice because larger block sizes create too many collisions.

7. Consider a RAID-5 system with four data blocks (b_0, b_1, b_2, b_3) and one parity block p per stripe.

a. How much of the total disk space is used by parity blocks? (5 points) 20 percent

b. How can we reconstitute the contents of block b_3 after the disk holding that block ***has failed***? (5 points)

$b_3 = b_0$ XOR b_1 XOR b_2 XOR p

8. Assuming that a main memory access takes

1 bus clock cycle to send the address,

16 bus clock cycle to initiate a read,

1 bus clock cycle to send a word of data,

how many clock cycles would it take to transfer 16 bytes to the cache if

a. the data are stored in a ***single bank*** of memory? (5 points) **Answer:** **69 cycles**
(*You can use this space to detail your computation.*)

1 + 4×(16 + 1) = 69 (because all operations are done sequentially)

b. the data are stored in a ***four-way interleaved*** memory? (5 points) **Answer:** **21 cycles**
(*You can use this space to detail your computation.*)

1 + 16 + 4×1 = 21
(because the reads, but not the data transfers, are performed in parallel)

9. How can we prevent user programs from ***modifying their own page tables***? (5 points)

We must store page tables in the protected area of the operating system.

10. How can we protect the ***integrity and the security of user data on disk***? (5 points)

We need a dual-mode CPU that will distinguish between non-privileged instructions that all processes can execute and privileged instructions that only the kernel can execute. Making all I/O instructions privileged will prevent people form directly accessing the data on disk.