NAME: ________________________________ (FIRST NAME FIRST) **SCORE:** ________

COSC 3330 **FIRST MIDTERM** **FEBRUARY 22, 2010**

*This exam is **closed book**. You can have **one page** of notes. UH expels cheaters.*

1. Simplify the following Boolean expression. (10 points)

$$\mathbf{v\,w\,x + w\,(v\,x\,y + y) + w'\,y + y}$$

$v\,w\,x + w\,(v\,x\,y + y) + w'\,y + y =$

$v\,w\,x + v\,w\,x\,y + w\,y + w'\,y + y =$

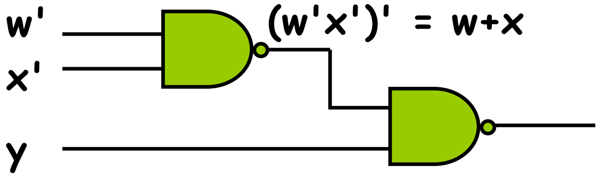
$v\,w\,x + y$

2. Give a simplified implementation for the following expression using only NAND gates. (20 points)

$$\mathbf{w\,x\,y' + w'\,(x \oplus y) + x'\,y'}$$

$$w\,x\,y' + w'\,(x \oplus y) + x'\,y' =$$
$$w\,x\,y' + w'\,(x\,y' + x'\,y) + x'\,y' =$$
$$w\,x\,y' + w'\,x'\,y + x'\,y' =$$
$$w\,x\,y' + x\,y' + w'\,x'\,y + x'\,y' =$$
$$w'\,x'\,y + y' =$$
$$w'x'y + y' + w'x'y' =$$
$$w'x' + y'$$

which we implement as $((w'x')'y)' = w'x' + y'$



$((w'x')'.y)' =$

$((w+x)\ .y')' =$

$w'x' + y'$

3. Consider a huge program that consists of a purely sequential part that takes one hour and another part that takes three hours. What is the ***maximum speedup*** we can achieve by parallelizing the second part of the program? (5 points)

The maximum speedup we can achieve is a factor of ___4______.

4. Server motherboard A has a SPEC CPU2006 rating of 31.4 while server B has a rating of 39.7. Which one of the two motherboards is faster? (5 points)

Motherboard _____B______.is faster than the other motherboard.

5. Assume we have a very basic microprocessor doing 4-bit arithmetic. (3×5 points)

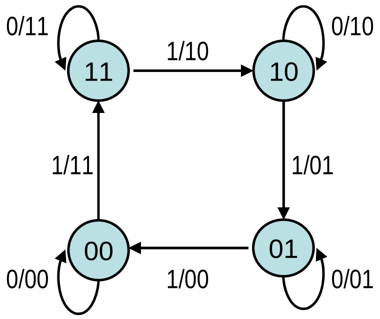
a. How would you represent the decimal value **– *7*** in ***signed arithmetic***? _________________1001

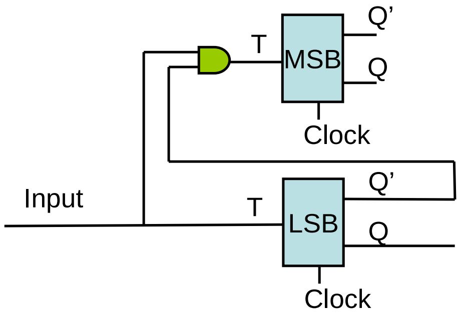
b. What would be its ***result of adding* 0100 to 0100** assuming that

i. The numbers being added were ***unsigned integers***? __________ 0100 +0100 = 1000 = 8_{ten}

ii. The numbers being added were ***signed integers***? ________ 0100 +0100 = 1000 = overflow

6. Implement a two-bit counter going to the cycle **00, 11, 10, 01, 00, …** when its input is on**.** You may use the flipflops and the gates of your choice. (15 points)





Two T flip-flops: one for the more significant bit and one for the less significant bit

Input of LSB flipflop: signal line
Input of MSB flipflop: signal line and complemented output of LSB flipflop

7. Given the following MIPS instructions, how would you

```
lw      r1, a(r2)
addi    r1, r2, #n
addiu   r1, r2, #n
andi    r1, r2, #n
ori     r1, r2, #n
```

a. Set the contents of register **r0** to **one**? (5 points)

ori r1, $0, 1 __OR__ addi r1, $0, 1 ____

b. Copy the contents of register **r1** into register **r0?** (5 points)

ori r0, r1, 0 __OR__ addi r0, r1, 0 ____

10. Unlike the IBM/360 instruction set, the MIPS instruction set has ***fixed-size*** instructions**.**

a. What is the main advantage of having ***fixed-size instructions***? (5 points)

It lets predict the exact location of an instruction before decoding the instructions that precede it and allows prefetching and pipelining

b. Which group of MIPS instructions takes advantage of this property and how? (5 points)

I-format jump instructions multiply their offset by 4 because all instructions are 4-byte wide.

11. Explain why the ***very large instruction set*** of the ***x86*** **family** of processors is at the same time a ***nightmare*** and a ***blessing*** for both Intel and AMD. (2×5 points)

- A *nightmare* to implement.
- A *blessing* because it discourages the competition.