NAME: ___KEY_____ (FIRST NAME FIRST) **SCORE**: _____

COSC 3330 SECOND MIDTERM APRIL 5, 2010

*This exam is **closed book**. You can have **one page** of notes. UH expels cheaters.*

1. For each of the following MIPS instructions, check the cycles that each instruction does not skip. (4×5 points for each correct line)

Instruction	*IF*	*ID/RR*	*ALU*	*MEM*	*WB*
add r1, r2, r3	X	X	X		X
slt r1, r2, r3	X	X	X		X
ld r1, d(r2)	X	X	X	X	X
st r1, d(r2)	X	X	X	X	

2. Which decimal values are stored in the following single precision floating point numbers? (2×5 points) (***Hint:*** 127_{ten} *is the value you need to use in your computation.*)

1	**129_{ten}**	**01000000000000 … 00000000000000**

Answer: $-1.01\times2^{2}=-101 = -5$

0	**124_{ten}**	**10000000000000 … 00000000000000**

Answer: $1.\ 1\times2^{-3}= 11\times2^{-4} = 3/16$

3. What is a ***denormalized number***? (5 points) What would be the possible value(s) of its ***exponent field***? (5 points)

A denormalized number is a number that is not normalized because it too small. It has no implicit 1 and its exponent is all zeroes

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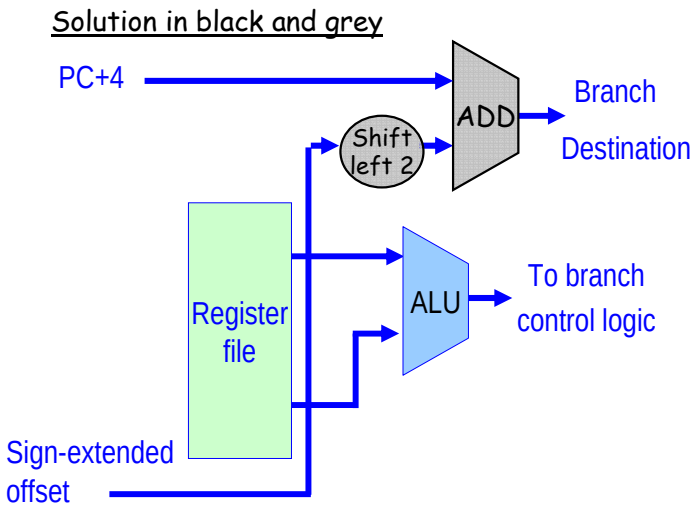
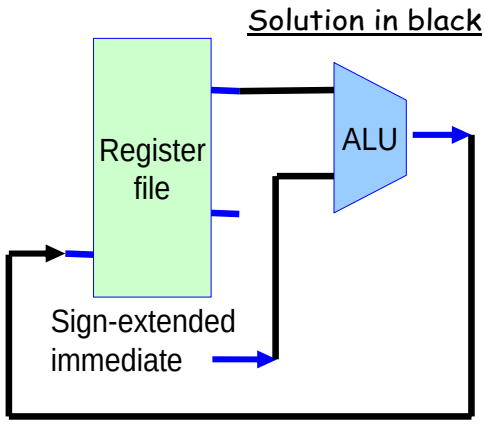
4. What is missing in the following diagram sketching the datapaths of the ***non-pipelined*** version of the ***conditional branch*** instruction? (2×5 points)



5. Remember that the MIPS instruction set has a variety of immediate instructions such as

addi r1, r2, im

that stores into **r1** the sum of the contents of register **r1** and the immediate value **im.** Show on the following diagram what would be the datapaths for that instruction. (3×5 points)



6. What do we mean when we say that disk failure rates follow a ***bathtub curve***? **(**5 points)

Disk failure rates are said to follow a bathtub curve because they are much higher (a) during the first few months after the disk is installed and (b) when it wears down at the end of its useful lifetime.

7. Consider the flowing pair of MIPS instructions

```
sub $t1, $s2,$t3
add $s1,$t1,$s4
```

a. Show how the second instruction will proceed when ***bypassing*** is ***not implemented***. (5 points)

Instruction	*Cycle* 0	*Cycle* 1	*Cycle* 2	*Cycle* 3	*Cycle* 4	*Cycle* 5
sub $t1, $s2,$t3	**IF**	**ID/RR**	**ALU**	**WB**		
add $s1,$t1,$s4		**IF**			**ID/RR**	**ALU**

b. Show how the second instruction will proceed if ***bypassing*** is ***implemented***. (5 points)

Instruction	*Cycle* 0	*Cycle* 1	*Cycle* 2	*Cycle* 3	*Cycle* 4	*Cycle* 5
sub $t1, $s2,$t3	IF	ID/RR	ALU	WB		
add $s1,$t1,$s4		IF	ID/RR	ALU	WB	

c. Which single MIPS instruction can cause the worst data hazards**?** (5 points)

Answer: lw (because it goes though all cycles before updating the register)

8. The MIPS architecture we have discussed in class includes a ***small comparator*** that checks whether the two register read outputs are equal or not.

a. Which MIPS instructions use this comparator**?** (5 points)

Answer: beq and bne

Why do they use this comparator instead of the ALU**?** (5 points)

To reduce control hazards by deciding faster whether the branch should be taken or not.

b. How is this comparator implemented? (5 points)

It XORes the two 32 values then ORes bitwise the result.