## Due Wednesday, September 19 IN CLASS

1. Consider a program consisting of two parts, namely one part that is purely sequential and takes 64 s to complete and another part that takes $1,024 \mathrm{~s}$ when run on a uniprocessor architecture. Assume that this second part can be easily decomposed into two or more parallel tasks and that speedup thus obtained is inversely proportional to the number of tasks executing in parallel. As a result, the parallel part of the program would only take 512 s to run on a dual processor architecture, 256 s to run on a quad processor architecture and so on.
a) What would be the speedups that the program would achieve if it was to run on computers with 2 , $4,8,16$, and 32 processors? ( $4 \times 4$ easy points)
b) What would be the maximum speedup that the program would achieve if it was to run on a computer with an unlimited number of processors? (4 easy points)
2. Simplify the two following logical expressions:

$$
\begin{aligned}
& \text { ABC'D' + AB'D' + ACD + CD } \\
& (\mathbf{A} \oplus \mathbf{B C})(\mathbf{B}+\mathbf{A})
\end{aligned}
$$

using both algebra and Karnaugh maps. (20 points)
3. Simplify the expression $(\mathbf{A B C})^{\prime}(\mathbf{A}+\mathbf{D E})^{\prime}(\mathbf{A} \oplus \mathbf{B C})(\mathbf{B}+\mathbf{E})$ and convert it to a form that can be represented using a programmable logic array. (20 points)
4. Implement the double implication operation, $\mathbf{A} \Leftrightarrow \mathbf{B}=\mathbf{A B}+\mathbf{A}^{\prime} \mathbf{B}$ ', using only NAND gates. (10 points)
5. Build a regular $\mathbf{D}$ flip-flop using an $\mathbf{R}$ ' $\mathbf{S}^{\prime}$ latch, that is, an $\mathbf{R S}$ latch with inverted values for $\mathbf{R}$ and $\mathbf{S}$, and as few NOR gates as possible. (10 points)
6. Build a synchronous sequential circuit with two inputs, respectively named P-for plus-and M-for minus-and two outputs respectively named O-for overflow-and U—for underflow. The circuit state transitions are:
a) When $\mathrm{P}=\mathrm{M}=0$, the system remains in its current state.
b) When $\mathrm{P}=1$ and $\mathrm{M}=0$, the system possible transitions are:

- $000 \rightarrow 001 \rightarrow 010 \rightarrow 011 \rightarrow 100 \rightarrow 101 \rightarrow 110 \rightarrow 111 \rightarrow 000$
c) When $\mathrm{P}=0$ and $\mathrm{M}=1$, the system possible transitions are:
- $000 \rightarrow 111 \rightarrow 110 \rightarrow 101 \rightarrow 100 \rightarrow 011 \rightarrow 010 \rightarrow 001 \rightarrow 000$
d) We will never have $\mathrm{P}=\mathrm{M}=1$.

The O and U outputs are normally equal to zero except that
a) O is equal to one when there is a P transition from 111 to 000 (transition $\mathrm{P} / 10$ ).
b) U is equal to 1 when there is an M transition from 000 to 111 (transition $\mathrm{M} / 01$ ). (20 points)


