COSC 3330/6308 SECOND PROBLEM SET FALL 2012

Due Wednesday, October 24, 2012 IN CLASS

1. Detail for each of the four following MIPS instructions, which actions are being taken at each of their five steps. Do not forget to mention how and during which steps each instruction updates the program counter. (4×10 points)**.**

a) `jalr $s0, $s1`

b) `sw $s1, 24($t0)`

c) `slt $t0, $s3, $s4`

d) `jal 1048576`

2. Consider these two potential additions to the MIPS instruction set and explain how they would restrict pipelining. (2×5 easy points)

a) `cp d1(r1), d2(r2)`
copy contents of word at address contents of `r2` plus offset `d2` into address contents of `r1` plus displacement `d1`.

b) `incr d2(r2)`
adds one to the contents of word at address contents of `r2` plus offset `d2`.

3. Explain how you would pipeline the four following pairs of statements. (4×5 points)

a)
```
add $t0, $s0, $s1
beq $s1,$s2, 300
```

b)
```
add $t2, $t0, $t1
sw $t3, 36($t2)
```

c)
```
add $t0, $s0, $s1
beq $t0,$s2, 300
```

d)
```
lw $t0, 24($t1)
sub $s2, $t0, $t1
```

4. A computer system has a two-level memory cache hierarchy. The L1 cache has a zero hit penalty, a miss penalty of 5 ns and a hit rate of 95 percent. The L2 cache has a miss penalty of 100 ns and a hit rate of 90 percent.

a) How many cycles are lost by each instruction accessing the memory if the CPU clock rate is 2 GHz? (5 points)

b) We can either increase the hit rate of the topmost cache to 98 percent or increase the hit rate of the second cache to 95 percent. Which improvement would have more impact? (10 points)

5. A virtual memory system has a virtual address space of 4 Gigabytes and a page size of 8 Kilobytes. Each page table entry occupies 4 bytes.

a) How many bits remain unchanged during the address translation? (5 points)

b) How many bits are used for the page number? (5 points)

c) What is the maximum number of page table entries in a page table? (5 points)