Chapter 6

Flip-Flops and Simple Flip-Flop Applications

Basic bistable element

- It is a circuit having two stable conditions (states).
- It can be used to store binary symbols.

Flip-flops

A flip-flop is a bistable device, with inputs, that remains in a given state as long as power is applied and until input signals are applied to cause its output to change.

Latches vs. flip-flops

- Latches are flip-flops for which the timing of the output changes are not controlled.
- For a latch, the output essentially responds immediately to changes on the input lines (and possibly the presence of a clock pulse).
- A flip-flop is designed to change its output at the edge of a controlling clock signal.

SR (Set-Reset) latch

Next state

- If Q denotes the present state of a memory device, i.e., the state at the time the input signals are applied, we shall use Q+ or Q(t+1) to denote the next state, i.e., the new state assumed by the device in response to the input signals.
R’S’ latch

Gated SR latch

Gated D latch

Timing considerations

• Propagation delays
• Minimum pulse width
• Setup and hold time

Propagation delay
The time it takes a change in the input signal to produce a change in the output signal.

Minimum pulse width
The minimum amount of time a signal must be applied in order to produce a desired result.
Setup and hold times

- To achieve a satisfactory operation of a gated latch, constraints are normally placed on the time intervals between input changes.
- The minimum time the input signal must be held fixed before and after the latching action is called the setup time and hold time, respectively.

JK- and T-type flip-flops

In addition to the SR-type and D-type flip-flops discussed above, there are two other types, viz., JK- and T-type flip-flops.

JK flip-flops

A JK flip-flop works just like an SR flip-flop if we consider J input as S(et) input and K input as R(eset) input, except when both S and R inputs are set to 1, the output simply flips over.

T-type flip-flops

A T flip-flop is obtained from a JK flip-flop by tying the J and K inputs together to form the T input.

Flip-flops

- There are four different types of flip-flops: SR, D, JK, and T types.
- The properties of these flip-flops are summarized in the following 4 slides.
- The function and application tables are also known as characteristic and excitation tables, respectively.
**SR-type flip-flop**

- **Graphic symbol**
- **Characteristic equation**
  \[ Q(t+1) = S + R'Q \]

<table>
<thead>
<tr>
<th>S</th>
<th>R</th>
<th>Q(t+1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Q</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>?</td>
</tr>
</tbody>
</table>

**Function table**

**Application table**

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**D-type flip-flop**

- **Graphic symbol**
- **Characteristic equation**
  \[ Q(t+1) = D \]

<table>
<thead>
<tr>
<th>D</th>
<th>Q(t+1)</th>
<th>D</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
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<td>1</td>
<td>1</td>
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<td>1</td>
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<td>1</td>
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<td>1</td>
</tr>
</tbody>
</table>

**Function table**

**Application table**

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**JK-type flip-flop**

- **Graphic symbol**
- **Characteristic equation**
  \[ Q(t+1) = JQ' + K'Q \]

<table>
<thead>
<tr>
<th>J</th>
<th>K</th>
<th>Q(t+1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Q</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
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<tr>
<td>1</td>
<td>1</td>
<td>?</td>
</tr>
</tbody>
</table>

**Function table**

**Application table**

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**T-type flip-flop**

- **Graphic symbol**
- **Characteristic equation**
  \[ Q(t+1) = TQ' + T'Q \]

<table>
<thead>
<tr>
<th>T</th>
<th>Q(t+1)</th>
<th>T</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Q</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
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</tr>
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<td>1</td>
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<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

**Function table**

**Application table**

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**Positive and negative edge**

- The transition of a control signal (clock pulse) from its low to high value (0 to 1) in positive logic is called the **positive edge** of the control signal, while the transition from high to low (1 to 0) is called the **negative edge**.

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**Edge-triggered flip-flops**

- Edge triggered flip-flops use just one of the edges of the clock pulse to affect the reading of the input lines.
- These flip-flops are designed to be triggered by either the positive or negative edge.
- In analyzing the behavior of an asynchronous sequential circuit, one often needs to know which edge trigger the flip-flops used.
Serial-in, serial-out unidirectional shift register

Serial-in, parallel-out unidirectional shift register

Parallel-in unidirectional shift register

Universal shift register

4-bit binary ripple (asynchronous) counter with positive-edge triggered flip-flops.
A 3-bit up-counter

(a) Circuit

(b) Timing diagram

The flip-flops are triggered by positive going edge of the clock input.

Analysis method:
Construct a list of state changes as follows.
1. Assume that the counter starts with some values, say, 000.
2. Because \( T = 1 \) for \( Q_0 \), \( Q_0 \) will change at the arrival of every clock pulse.
3. Complete the listing for \( Q_0 \).
4. Because \( T = Q_0' \), and because the flip-flop is triggered by a positive going clock input, for \( Q_1 \), \( Q_1 \) changes its content whenever \( Q_0 \) changes from 1 to 0.
5. Do the same for the listing for \( Q_2 \).

A 3-bit down-counter

(a) Circuit

(b) Timing diagram

The flip-flops are triggered by positive going edge of the clock input.

Analysis method:
Construct a list of state changes as follows.
1. Assume that the counter starts with some values, say, 000.
2. Because \( T = 1 \) for \( Q_0 \), \( Q_0 \) will change at the arrival of every clock pulse.
3. Complete the listing for \( Q_0 \).
4. Because \( T = Q_0 \), and because the flip-flop is triggered by a positive going clock input, for \( Q_1 \), \( Q_1 \) changes its content whenever \( Q_0 \) changes from 0 to 1.
5. Do the same for the listing for \( Q_2 \).

The following synchronous counter can be analyzed similarly.

Four-bit synchronous binary counter
Four-bit synchronous binary counter variation

Synchronous mod-10 counter

Mod-4 ring counter

Mod-8 twisted-ring counter (or Johnson counter)
Control signal generators

- A control signal generator is a sequential circuit that generate a sequence of bit patterns, each of which contains only one 1. It is used to activate various devices in turn.
- Shown in the next slide are the wave forms of 4-bit control signals.

Control-signal generator (continued)

There are three ways to generate control signals (with n bits):
1. Use an n-bit ring counter (need n flip-flops)
2. Use a binary counter and a decoder (need k flip-flops and n AND gates with k inputs, where n ≤ 2^k)
3. Use a Johnson counter (need n/2 flip-flops) and n 2-input AND gates.
A synchronous counter is a special kind of synchronous sequential circuit, the analysis and design of such a circuit will be discussed in the next chapter.

Counting sequence of a 3-bit Johnson counter

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
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<td>0</td>
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<td>0</td>
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</tbody>
</table>

A Johnson counter, augmented with a bank of AND gates, becomes a control-signal generator.