Chapter 6

Flip-Flops and Simple Flip-Flop Applications

Basic bistable element

- It is a circuit having two stable conditions (states).
- It can be used to store binary symbols.

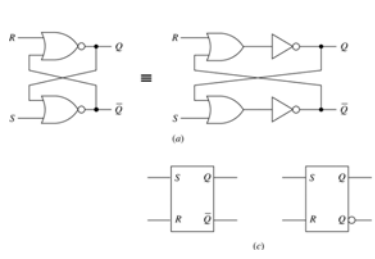
Flip-flops

A flip-flop is a bistable device, with inputs, that remains in a given state as long as power is applied and until input signals are applied to cause its output to change.

Latches vs. flip-flops

- Latches are flip-flops for which the timing of the output changes are not controlled.
- For a latch, the output essentially responds immediately to changes on the input lines (and possibly the presence of a clock pulse).
- A flip-flop is designed to change its output at the edge of a controlling clock signal.

SR (Set-Reset) latch



Inputs		Outputs	
S	R	Q^+	$\bar{Q}^+$
0	0	Q	$\bar{Q}$
0	1	0	1
1	0	1	0
1	1	0*	0*

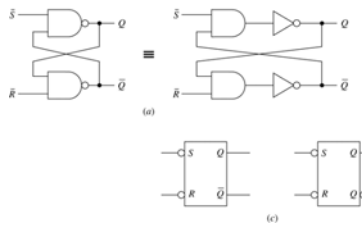
*Unpredictable behavior will result if inputs return to 0 simultaneously

(b)

Next state

- If Q denotes the present state of a memory device, i.e., the state at the time the input signals are applied, we shall use Q^+ or Q(t+1) to denote the *next state*, i.e., the new state assumed by the device in response to the input signals.

R'S' latch

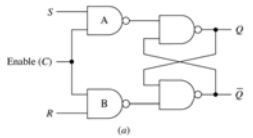


Inputs		Outputs	
$\bar{S}$	$\bar{R}$	Q^*	$\bar{Q}^*$
0	0	1*	1*
0	1	1	0
1	0	0	1
1	1	Q	$\bar{Q}$

*Unpredictable behavior will result if inputs return to 1 simultaneously

(b)

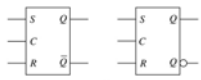
Gated *SR* latch



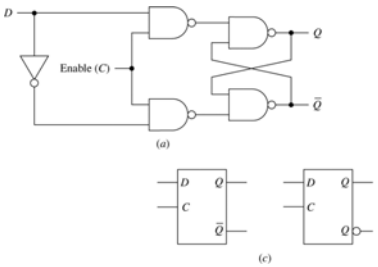
Inputs			Outputs	
S	R	C	Q^*	$\bar{Q}^*$
0	0	1	Q	$\bar{Q}$
0	1	1	0	1
1	0	1	1	0
1	1	1	1*	1*
X	X	0	Q	$\bar{Q}$

*Unpredictable behavior will result if S and R return to 0 simultaneously or C returns to 0 while S and R are 1

(b)



Gated *D* latch



Inputs		Outputs	
D	C	Q^*	$\bar{Q}^*$
0	1	0	1
1	1	1	0
X	0	Q	$\bar{Q}$

(b)

Timing considerations

- Propagation delays
- Minimum pulse width
- Setup and hold time

Propagation delay

The time it takes a change in the input signal to produce a change in the output signal.

Minimum pulse width

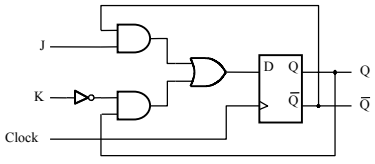
The minimum amount of time a signal must be applied in order to produce a desired result.

Setup and hold times

- To achieve a satisfactory operation of a gated latch, constraints are normally placed on the time intervals between input changes.
- The minimum time the input signal must be held fixed before and after the latching action is called the *setup* time and *hold* time, respectively.

JK- and T-type flip-flops

In addition to the SR-type and D-type flip-flops discussed above, there are two other types, viz., JK- and T-type flip-flops.

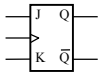


(a) Circuit

JK flip-flop

J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	Q̄(t)

(b) Truth table



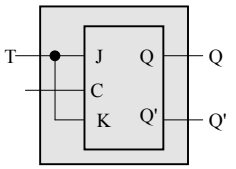
(c) Graphical symbol

JK flip-flops

A JK flip-flop works just like an SR flip-flop if we consider J input as S(et) input and K input as R(eset) input, except when both S and R inputs are set to 1, the output simply flips over.

T-type flip-flops

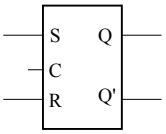
A T flip-flop is obtained from a JK flip-flop by tying the J and K inputs together to form the T input.



Flip-flops

- There are four different types of flip-flops: SR, D, JK, and T types.
- The properties of these flip-flops are summarized in the following 4 slides.
- The *function* and *application tables* are also known as *characteristic* and *excitation tables*, respectively.

SR-type flip-flop



Graphic symbol

$Q(t+1) = S + R'Q$

$SR = 0$

Characteristic equation

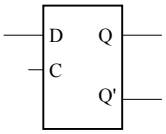
S	R	Q(t+1)
0	0	Q
0	1	0
1	0	1
1	1	?

Function table

Q	Q(t+1)	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

Application table

D-type flip-flop



Graphic symbol

$Q(t+1) = D$

Characteristic equation

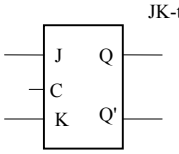
D	Q(t+1)
0	0
1	1

Function table

Q	Q(t+1)	D
0	0	0
0	1	1
1	0	0
1	1	1

Application table

JK-type flip-flop



Graphic symbol

$Q(t+1) = JQ' + K'Q$

Characteristic equation

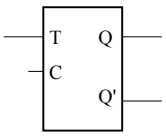
J	K	Q(t+1)
0	0	Q
0	1	0
1	0	1
1	1	Q'

Function table

Q	Q(t+1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Application table

T-type flip-flop



Graphic symbol

$Q(t+1) = TQ' + T'Q$

Characteristic equation

T	Q(t+1)
0	Q
1	Q'

Function table

Q	Q(t+1)	T
0	0	0
0	1	1
1	0	1
1	1	0

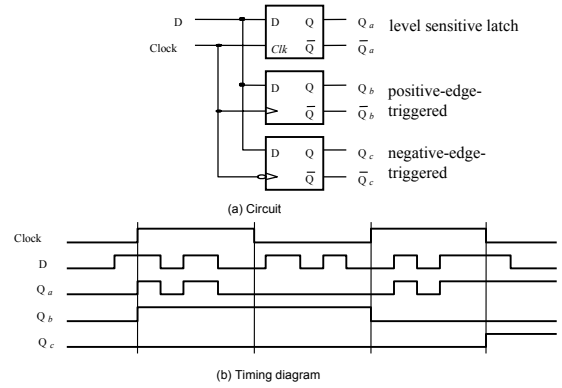
Application table

Positive and negative edge

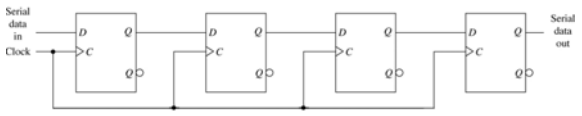
- The transition of a control signal (clock pulse) from its low to high value (0 to 1) in positive logic is called the *positive edge* of the control signal, while the transition from high to low (1 to 0) is called the *negative edge*.

Edge-triggered flip-flops

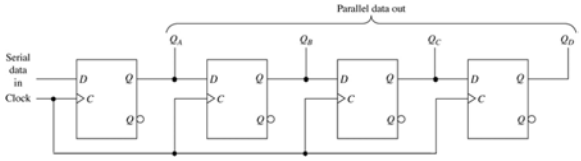
- Edge triggered flip-flops use just one of the edges of the clock pulse to affect the reading of the input lines.
- These flip-flops are designed to be triggered by either the positive or negative edge.
- In analyzing the behavior of an asynchronous sequential circuit, one often needs to know which edge trigger the flip-flops used.



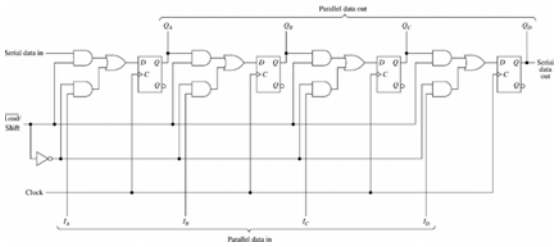
Serial-in, serial-out unidirectional shift register



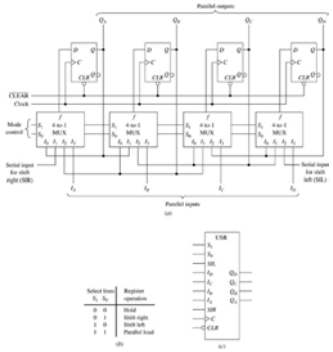
Serial-in, parallel-out unidirectional shift register



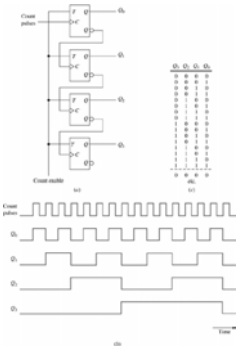
Parallel-in unidirectional shift register



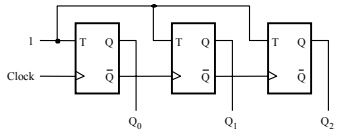
Universal shift register



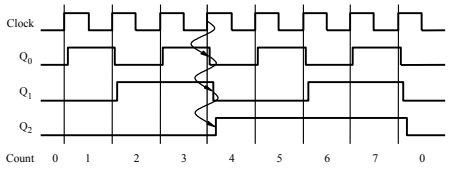
4-bit binary ripple (asynchronous) counter with positive-edge triggered flip-flops.



A 3-bit up-counter



(a) Circuit



(b) Timing diagram

The flip-flops are triggered by positive going edge of the clock input.

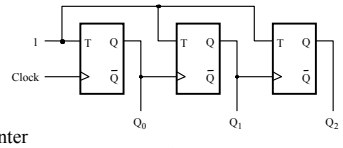
Analysis method:

Construct a list of state changes as follows.

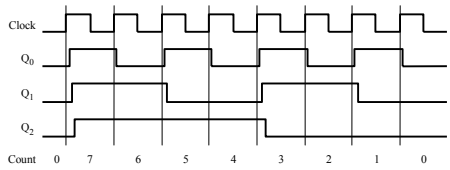
1. Assume that the counter starts with some values, say, 000.
2. Because T=1 for Q_0, Q_0 will change at the arrival of every clock pulse. Complete the listing for Q_0.
3. Because T=Q_0', and because the flip-flop is triggered by a positive going clock input, for Q_1, Q_1 changes its content whenever Q_0 changes from 1 to 0.
4. Do the same for the listing for Q_2.

Q_2	Q_1	Q_0
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1
0	0	0

A 3-bit down-counter



(a) Circuit



(b) Timing diagram

The flip-flops are triggered by positive going edge of the clock input

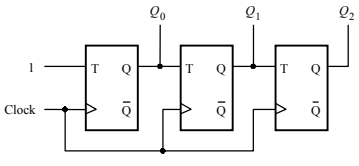
Analysis method:

Construct a list of state changes as follows.

1. Assume that the counter starts with some values, say, 000.
2. Because T=1 for Q_0, Q_0 will change at the arrival of every clock pulse. Complete the listing for Q_0.
3. Because T=Q_0, and because the flip-flop is triggered by a positive going clock input, for Q_1, it changes its content whenever Q_0 changes from 0 to 1.
4. Do the same for the listing for Q_2.

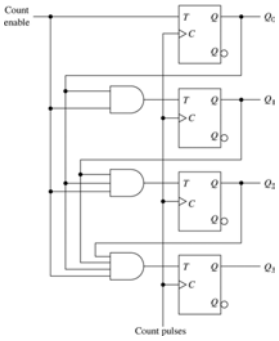
Q_2	Q_1	Q_0
0	0	0
1	1	1
1	1	0
1	0	1
1	0	0
0	1	1
0	1	0
0	0	1
0	0	0

The following synchronous counter can be analyzed similarly

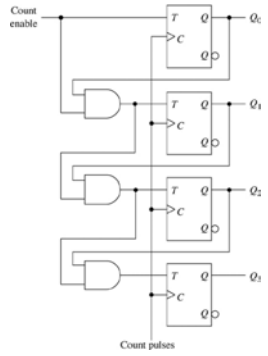


Q_2	Q_1	Q_0
0	0	0
0	0	1
0	1	0
1	1	1
0	0	0

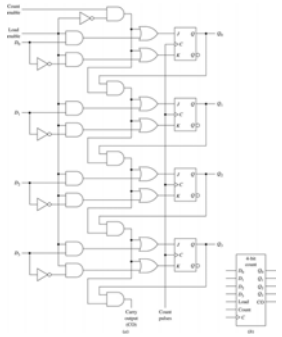
Four-bit synchronous binary counter



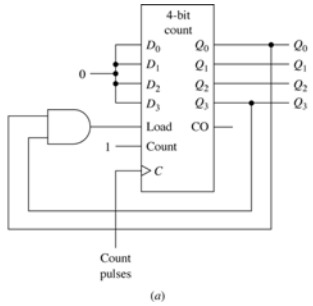
Four-bit synchronous binary counter variation



Four-bit synchronous binary counter with parallel load inputs



Synchronous mod-10 counter

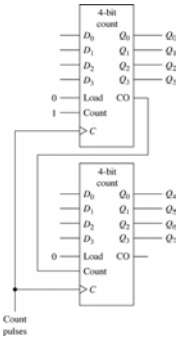


Q_3	Q_2	Q_1	Q_0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
0	0	0	0

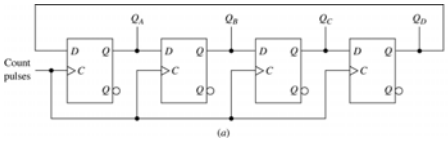
etc.

(b)

8-bit synchronous binary counter constructed from two 4-bit synchronous binary counters



Mod-4 ring counter

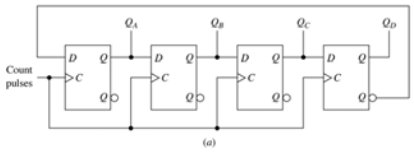


Q_A	Q_B	Q_C	Q_D
1	0	0	0
0	1	0	0
0	0	1	0
0	0	0	1
1	0	0	0

etc.

(b)

Mod-8 twisted-ring counter (or Johnson counter)

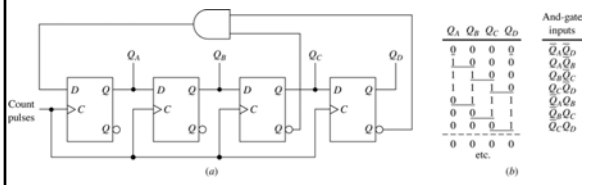


Q_A	Q_B	Q_C	Q_D	And-gate inputs
0	0	0	0	$\overline{Q}_A\overline{Q}_D$
1	0	0	0	Q_AQ_B
1	1	0	0	Q_BQ_C
1	1	1	0	Q_CQ_D
1	1	1	1	Q_AQ_D
0	1	1	1	$\overline{Q}_AQ_B$
0	0	1	1	$\overline{Q}_BQ_C$
0	0	0	1	$\overline{Q}_CQ_D$
0	0	0	0	

etc.

(b)

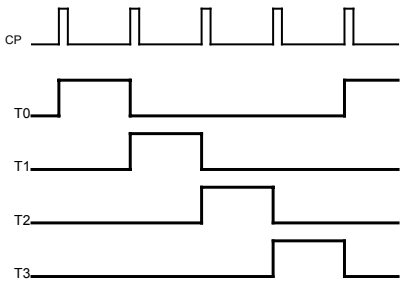
Mod-7 twisted-ring counter



Control signal generators

- A control signal generator is a sequential circuit that generate a sequence of bit patterns, each of which contains only one 1. It is used to activate various devices in turn.
- Shown in the next slide are the wave forms of 4-bit control signals.

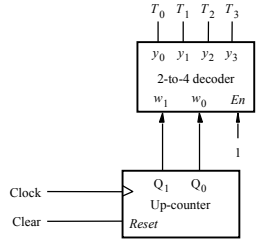
4-bit control pulses



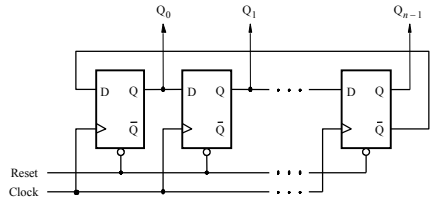
Control-signal generator (continued)

There are three ways to generate control signals (with n bits):

1. Use an n-bit ring counter (need n flip-flops)
2. Use a binary counter and a decoder (need k flip-flops and n AND gates with k inputs, where $n \leq 2^k$)
3. Use a Johnson counter (need n/2 flip-flops) and n 2-input AND gates.



A part of the control circuit for the processor



An n-bit Johnson counter, augmented with 2n AND-gates, will generate 2n-bit control signals. It uses n/2 flip-flops, 2n 2-input, AND gates.

Figure 7.30 Johnson counter

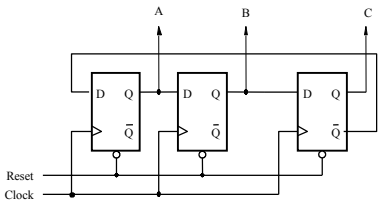
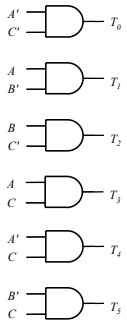


Figure 7.30 A 3-bit Johnson counter

Counting sequence of a 3-bit Johnson counter

A	B	C
0	0	0
1	0	0
1	1	0
1	1	1
0	1	1
0	0	1
0	0	0



A Johnson counter, augmented with a bank of AND gates, becomes a control-signal generator

Synchronous counters

A synchronous counter is a special kind of synchronous sequential circuit, the analysis and design of such a circuit will be discussed in the next chapter.